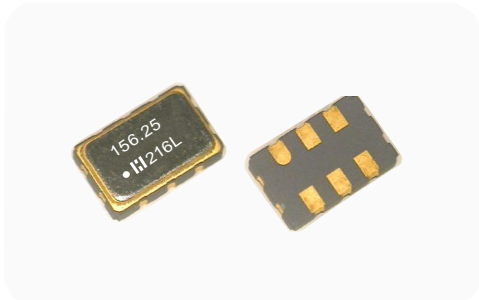


## D5SL Series

## 5032 HCSL OSC



### FEATURES

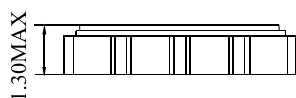
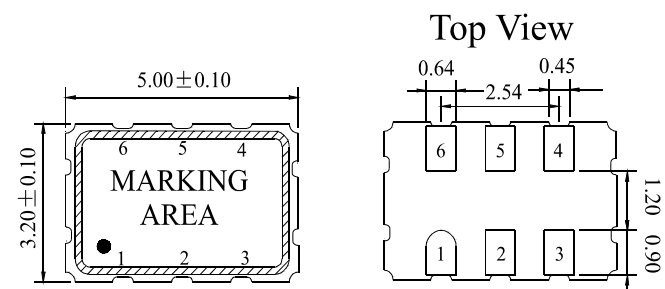
- 5.0\*3.2\*1.3mm package
- Tri-State function available
- Low Jitter and Noise
- HCSL output
- Ideal for Fiber-optic communication applications, FTTH and SONET/SDH applications, Sever, FCHBA, Fibre Channel, Gigabit Ethernet, and Serial ATA

### Electrical Specifications

Parameter	Condition	D5SL
Frequency Range	F0	25~156.25MHz
Output Specification		HCSL
Frequency Stability*	All Condition	±25ppm, ±50ppm, ±100ppm
Operating Temperature Range	T <sub>OPR</sub>	-20°C~+70°C(-40°C~+85°C option)
Storage Temperature Range	T <sub>STG</sub>	-55°C~+125°C
Power supply Voltage	V <sub>DD</sub>	3.3V+/-5%      2.5V+/-5%
Supply Current	I <sub>DD</sub>	90mA Max
Output Symmetry	Sym	At ½V <sub>pp</sub> 40/60%(45/55% Option)
Rise time	T <sub>r</sub>	20%V <sub>pp</sub> ~80%V <sub>pp</sub> 1nS Max
Fall Time	T <sub>f</sub>	80%V <sub>pp</sub> ~20%V <sub>pp</sub> 1nS Max
Output Voltage	V <sub>OH</sub> V <sub>OL</sub>	0.74V Typ. 0V Typ.
Output Load		50 ohm
Integrated phase jitter (RMS)	Integrated 12KHz to 20MHz	1pS Max
Start Time	T <sub>s</sub>	10mS Max
Aging(First Year)	25°C ±3°C	±2ppm Max
Pin 1,tri-state function		Pin 1=H or open....Output active at pin 4,5 Pin 1=L.....high impedance at pin 4,5
Packing Unit		3000pcs/reel

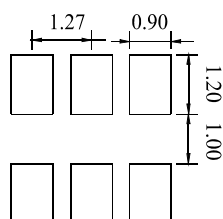
\*Include: 25°C tolerance, operating temperature range, input voltage change, aging, load change, shock and vibration

### Mechanical Dimensions(mm)

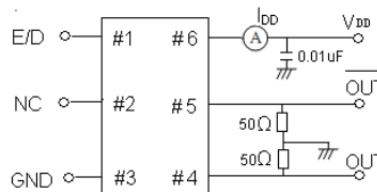


Pin	Connection
#1	Tri-State
#2	N.C.
#3	GND
#4	Comp. Output
#5	Out
#6	V <sub>DD</sub>

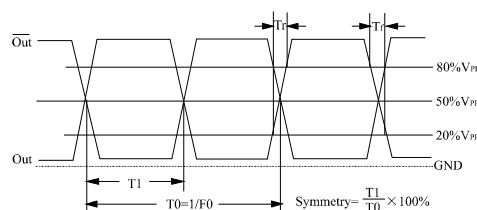
### Recommended Solder Pattern



### Test Circuit



### Output Waveform



\*\*Note: 0.01uF bypass capacitor should be placed between V<sub>DD</sub>(Pin6) and GND(Pin3) to Minimize power supply line noise