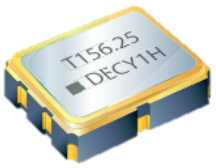
Product Features

1. Output Frequency：15~2100 MHz
2. Frequency Stability ：
   ± 30 ppm @ (-40 ~ 85℃)
   ± 50 ppm @ (-40 ~ 105℃)
3. Supply Voltage ： 1.8 , 2.5 , 3.3V (Typ.)
4. Output Type ： LVDS
5. High Power Supply Noise Rejection Performance
6. Industry Standard Package：
   7.0 x 5.0 x 1.7 mm (BG Series)

Application：

- Optical Modules
- High Speed Network Interface Cards
- Data Center Switch



RoHS COMPLIANT
REACH COMPLIANT
Pb Free
Halogen Free HF

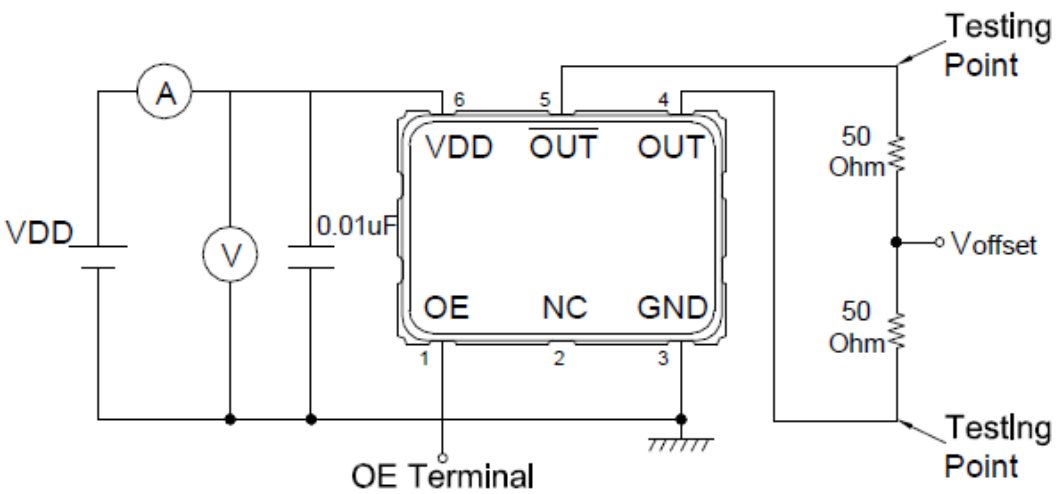
Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

- **Table 1 . Electrical Specifications**

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions & Notes
Nominal Frequency	F	15~2100			MHz	LVPECL / LVDS /CML
		15~700				HCSL
Frequency Stability	ST	± 30			ppm	@ -40~85℃ , Note 1
		± 50				@ -40~105℃ , Note 1
Operating Temperature	Topr	-40	-	85	℃	
		-40	-	105		
Supply Voltage	Vdd	1.8 , 2.5 , 3.3 (± 10%)			V	
Symmetry	TH/T	45	50	55	%	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
Current Consumption	Icc	-	69	80	mA	RL=100Ω
Standby Current	Icc(ST)	-	67	78	uA	OE = Low
Offset Voltage	-	1.125	1.250	1.375	V	
Output Swing (Single)	-	247	330	454	mV	Single Peak-to-Peak
Output Swing (Differential)	Vdiff	494	660	908	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.35	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7xVdd	-	-	V	Note 2
Enable Voltage Low	-	-	-	0.3xVdd	V	Note 2
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.15	0.25	ps	Integrated from 12KHz ~ 20MHz @150MHz , 3.3V , Note 3

Note 1 : Inclusive of frequency tolerance at 25℃ , variation over temperature , supply voltage variation , 10 years aging and vibration.
Note 2 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.
Note 3 : Phase Jitter will be slightly different according to output frequency and supply voltage.

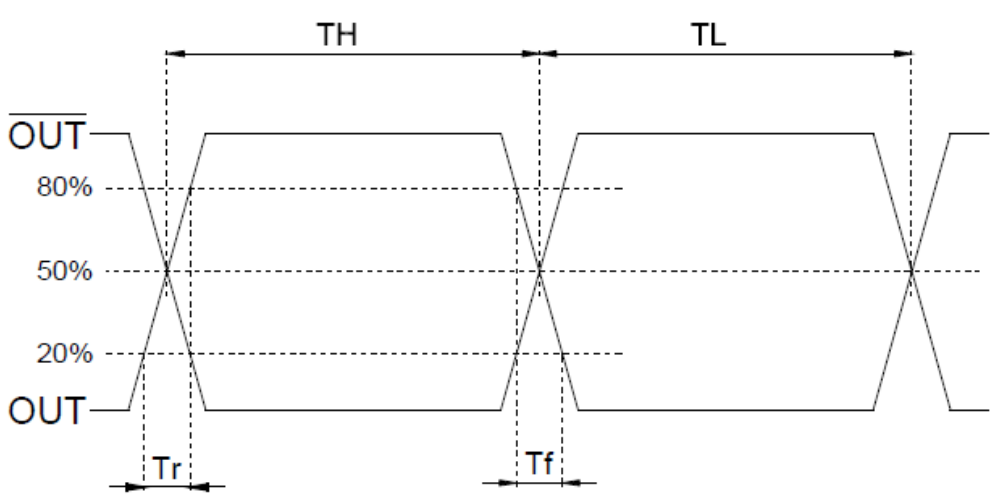
- **Test Diagram**



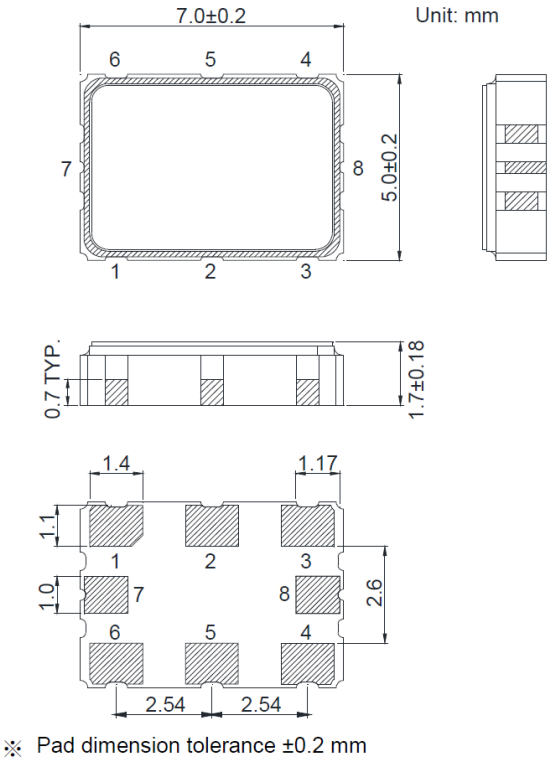
Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All of the testing equipment are 50 Ohm terminal.
3. OE terminal is open connection except OE function test.

- **Waveform Conditions**



- **Dimensions & Footprint(Recommended)**

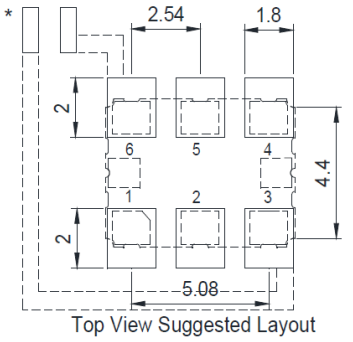


※ Pad dimension tolerance ±0.2 mm

Pin Function:

1. OE	7. NC
2. NC	8. NC
3. GND	
4. OUT	
5. $\overline{\text{OUT}}$	
6. VDD	

Land Pattern:



Top View Suggested Layout

※ Power Supply Decoupling Capacitor is Required.

※ Pad dimension tolerance ±0.2 mm