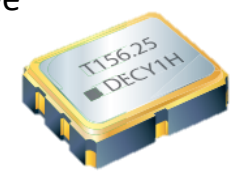
Product Features

1. 6 pads seam sealed ceramic package
2. 3.3 and 2.5 V operation available
3. Output Type : LVPECL
4. Output frequencies 50MHz ~ 320MHz
5. Excellent low phase noise and jitter
6. Tri-State function available
7. RoHS and REACH Compliant , Pb-free , Halogen-free
8. Industry Standard Package：
   3.2 x 2.5 x 0.95 mm

Application：

- Fiber Channel , Gigabit Ethernet , Serial ATA , Serial Attached SCSI , PCI-Express , SDH / SONET , Ethernet Switch
- Telecom , Networking , Server , Storage , Instrument



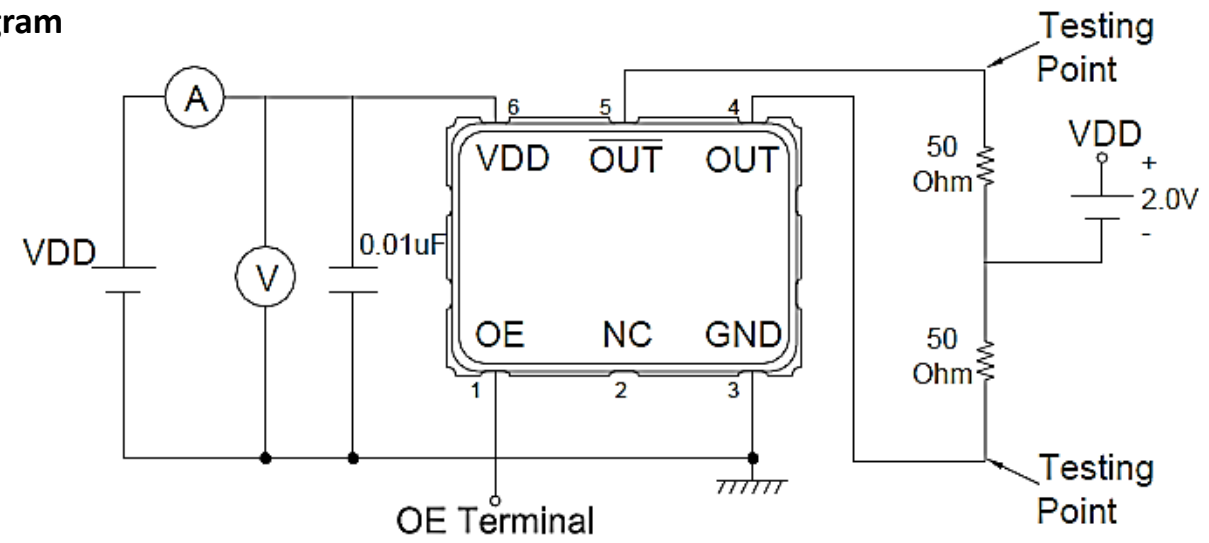
Test condition
Ambient temperature：25 ± 5°C
Relative humidity： 40% ~ 70%

- **Table 1 . Electrical Specifications**

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions & Notes
Common Electrical Characteristics						
Nominal Frequency	F	50 ~ 320			MHz	3rd Overtone
Frequency Stability	ST	± 25			ppm	@ -40~85°C , Note 1
		± 30				@ -40~105°C , Note 1
		± 50				@ -40~125°C , Note 1
Operating Temperature	Topr	-40	-	125	°C	
Supply Voltage	Vdd	2.25 ~ 3.63			V	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
LVPECL Electrical Characteristics						
Current Consumption	Icc	-	-	80	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	-	10	uA	OE = Low
Output Voltage High	VoH	VDD-1.025	-	VDD-0.88	V	
Output Voltage Low	VoL	VDD-1.81	-	VDD-1.62	V	
Output Voltage Range	Vdiff	600	1400	2000	mV	Differential Peak-to-Peak
Rise Time	Tr	-	-	0.5	ns	20% ~ 80% Output Swing
Fall Time	Tf			0.5	ns	80% ~ 20% Output Swing
Symmetry	TH/T	45	50	55	%	
Enable Voltage High	-	0.7VDD	-	-	V	Note 2 , (Logic 1)
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2 , (Logic 0)
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.1	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note3

Note 1 : Inclusive of frequency tolerance at 25°C , variation over temperature , supply voltage variation , 10 years aging and vibration.
Note 2 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.
Note 3 : Phase Jitter will be slightly different according to output frequency and supply voltage.

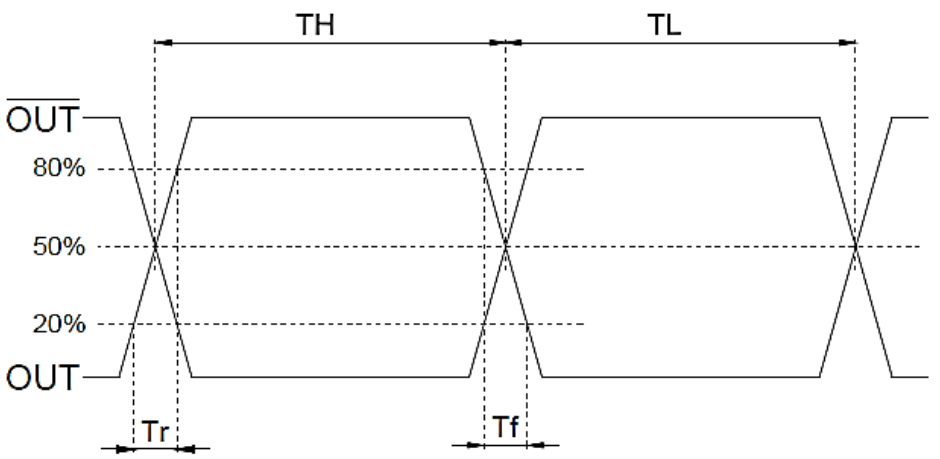
- **Test Diagram**



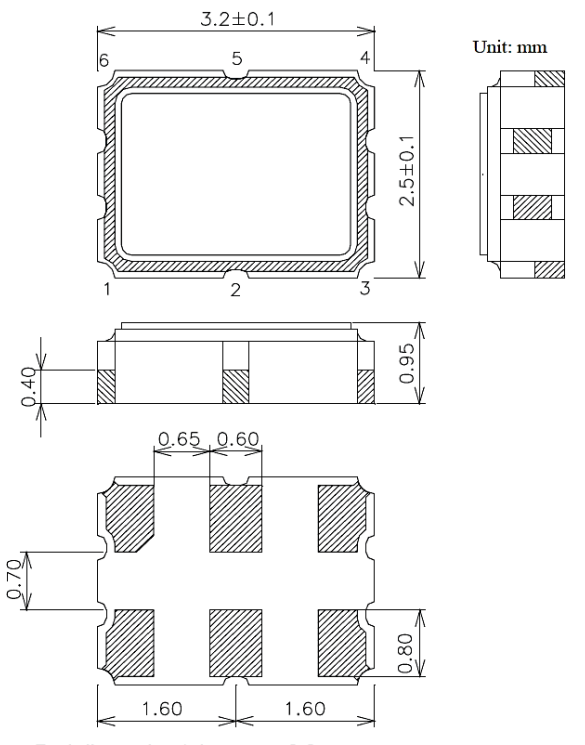
Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All the testing equipment are 50 Ohm terminal.
3. OE terminal is open connection except OE function test.

- **Waveform Conditions**



- **Dimensions & Footprint (Recommended)**

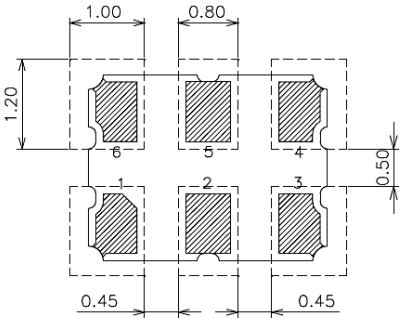


※ Pad dimension tolerance ±0.2 mm

Pin Function:

1. OE
2. NC
3. GND
4. OUT
5. $\overline{\text{OUT}}$
6. VDD

Land Pattern:



※ Power Supply Decoupling Capacitor is Required.